II. REMARKS

This paper is submitted in Response to the Office Action mailed on November 26, 2003. By the foregoing amendment, claims 13-16 and 19-20 have been amended. Claim 12 has been canceled. Claims 1-11 and 13-20 are pending in the Application. Reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

As a preliminary matter, Applicants acknowledge with appreciation the indication of allowable subject matter in claims 2-3, 6-7, 14, and 16-18. By the foregoing amendments, claims 14 and 16 have been amended to place them in independent form, including the limitations of their base and intervening claims. Applicants respectfully submit that claims 14 and 16 are now in condition for allowance, which action is earnestly solicited. As claim 16 is in condition for allowance, Applicants asserts that dependent claims 17-18 are also in condition for allowance, which action is earnestly solicited.

The following remarks address the merits of the Office Action that require response.

A. Objection to Claim 20

At paragraph 6 on page 4 of the Office Action mailed November 26, 2003, the Examiner objects to claim 20 on the basis of informalities. Claim 20 has been amended to overcome the objection. No further response is necessary at this time.

B. **Rejection of Claims 1, 4-5, 8, 11, 13, 15 and 19-20 under 35 U.S.C. § 102(e) as anticipated by Ooshi, *et al.*, and claims 9 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Ooshi, *et al.***

The Examiner rejects claims 1, 4-5, 8, 11, 13, 15 and 19-20 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,166,990 to Ooshi, *et al.*, and claims 9 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Ooshi *et al.* Applicants respectfully traverse the Examiner's rejection.

With regard to claim 1, the Examiner indicates that the Ooshi, *et al.* patent discloses each and every limitation of claim 1, including a synchronous dynamic memory "operating in synchronized with an external clock . . . wherein said clock input buffer supplies said internal clock to said command input buffer and stops supply of said internal clock to said address input buffer or data input buffer in data hold mode [*in power-down mode, inhibition of generation of internal clock signal causes the operation of the internal circuit to be halted; input buffer 5004 and the buffer circuits of address input circuit 5010 have their operation st*opped; col. 3, lines 26-43]." See, e.g., Office Action at pages 3-4.

Ooshi, *et al.* fails to disclose or suggest each and every limitation of claim 1, which is a requirement for making out a rejection under 35 U.S.C. § 102. See, MPEP § 2131. For example, Ooshi, *et al.* fails to teach or suggest at least the limitation of a clock input buffer that "supplies said internal clock to . . . said command input buffer and stops supply of said internal clock to said address input buffer or data input buffer in data hold mode," as claimed in claim 1. Ooshi, *et al.* only discloses that, in a power down mode, a power down mode designating signal PD from control circuit 5008 is

applied to internal clock generation circuit 5000, whereby generation of internal clock signal CLKin in internal clock generation circuit 5000 is stopped. In the synchronous semiconductor memory device, the internal circuit operates in synchronization with internal clock signal CLKin. Inhibition of generation of internal clock signal CLKin causes the operation of the internal circuit to be halted. Once the internal clock CLKin is stopped, the input buffer 5004 and the address input circuit 5010 cannot receive the supplied command CMD and address ADD signal so that the internal circuit is in complete power down mode.

By contrast, in the data hold mode of the present invention, the internal clock is not supplied to the address input buffer or the data input buffer; it is supplied to the command input buffer. In the data hold mode, therefore, the command input buffer is active and can receive command signals.

For at least this reason, Applicants submit that claim 1 is allowable over the cited prior art. As claim 1 is allowable, Applicants submit that claims 4 and 9, which depend from allowable claim 1, are likewise allowable over the cited prior art.

Similarly to as discussed above with regard to claim 1, Applicants submit that claims 5 and 11 are allowable over the cited prior art at least because the cited prior art does not disclose or suggest at least the feature of a clock input buffer that supplies an internal clock to the command input buffer and stops supplying the internal clock to the address input buffer or data input buffer in the data hold mode, as claimed in claims 5 and 11. As claim 5 is allowable, Applicants submit that claims 8-10, which depend from allowable claim 5, are likewise allowable over the cited prior art.

With regard to claim 13, Applicants submit that Ooshi, *et al.* does not teach or suggest at least the limitation of a clock buffer controller that monitors if there is a

change in the input signal and activates the clock buffer only when there a change is detected in the input signal, as claimed in claim 13, as amended. For at least this reason, Applicants submit that claim 13 is allowable over the cited prior art.

Similarly to as discussed above with regard to claim 13, Applicants submit that claims 15 and 19-20 are allowable over the cited prior art at least because the cited prior art does not disclose or suggest the at least the feature of a clock buffer controller that monitors if there is a change in the input signal and activates the clock buffer only when there a change is detected in the input signal, as claimed in claims 15 and 19-20, as amended.

With regard to each of the rejections under §103 in the Office Action, it is also respectfully submitted that the Examiner has not yet set forth a *prima facie* case of obviousness. The PTO has the burden under §103 to establish a *prima facie* case of obviousness. In re Fine, 5 U.S.P.Q.2nd 1596, 1598 (Fed. Cir. 1988). Both the case law of the Federal Circuit and the PTO itself have made clear that where a modification must be made to the prior art to reject or invalidate a claim under §103, there must be a showing of proper motivation to do so. The mere fact that a prior art reference could arguably be modified to meet the claim is insufficient to establish obviousness. The PTO can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. Id. In order to establish obviousness, there must be a suggestion or motivation in the reference to do so. See also In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984) (prior art could not be turned upside down without motivation to do so); In re Rouffet, 149 F.3d 1350 (Fed. Cir.

1998); In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Lee, 277 F.3d 1338 (Fed. Cir. 2002).

In the Office Action, the Examiner merely states that "the concept and advantages of using an LSI, wherein the synchronous dynamic memory is embedded on one chip with a processing circuit; and a memory controller that controls said synchronous dynamic memory are well known and expected in the art." See, e.g., Office Action at page 6. The Office Action concludes that it would have been obvious to modify Ooshi, *et al.* with the above LSI and memory controller "because it would have increased system performance by improving on the speed of data transfer between the logic section and the memory section. Id. Because there is no suggestion in the prior art to modify the reference, this is an insufficient showing of motivation.

For all of the above reasons, it is respectfully submitted that the claims now pending patentably distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300, referencing Attorney Docket No. 108066-00038. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300, referencing Attorney Docket No. 108066-00038.

Respectfully submitted,

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Enclosures: Petition for Extension of Time (one month)